Article

A MULTILEVEL CONVERTER WITH TRIPLE VOLTAGE BOOST FOR RENEWABLE ENERGY SOURCES

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Abstract

A compact, single-supply, multilevel inverter (SC-MLI) topology based on a switched-capacitor structure for high-efficiency power conversion is proposed. The overall goal of the study is to develop a three-stage inverter that increases the voltage by a factor of 13 while simultaneously reducing the number of required components. As a result, the proposed design reduces circuit complexity and cost while also increasing reliability. The inverter's performance was evaluated using theoretical analysis, MATLAB/Simulink and PLECS simulations, and experimental verification. In addition, tests using a natural capacitor without a control circuit or with resistive and inductive loads confirmed the stable generation of multi-level voltage and voltage balance with additional sensors. For example, when operating in sinusoidal pulse-width modulation (SPWM) and low-level control (NLC) modes, the inverter maintained low harmonic distortion and a uniform current waveform. As a result, the system achieved a maximum efficiency of 97.2% in modeling and 95.3% experimentally. The results of this study confirm the Recommended Level 13 SC-MLI compliance for renewable energy integration and other advanced power electronics applications.

Keywords: amplifier inverter; multi-level inverters (MLI); renewable energy use; self-balancing voltage; variable capacitor (SC)

I. Introduction

The growing use of renewable energy sources [1] and high-energy-density batteries has made multilevel converters (MLCs) increasingly popular in power electronics [2]. Modern systems require high efficiency, high power density, low harmonic distortion,

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and stable input voltage. Due to their structural advantages, MLCs enable high-quality DC–AC conversion and are widely used in electric vehicles, microgrids, charging infrastructures, and renewable-energy-based installations [3]. However, classical methods such as CHB, NPC, and FC require a large number of semiconductor components and independent power supplies, complicating circuit design and control [4]. Switched-capacitor (SC)-based topologies offer numerous advantages, such as compactness, lightweight design, high power density, and the elimination of the need for inductors for voltage conversion. These topologies make it possible for applications like multi-channel power supplies and voltage management [5,6]. These topologies also enable voltage step-up without the use of transformers, an advantage that distinguishes them from high-frequency magnetic systems [7,8]. Furthermore, capacitors are easier to use and significantly less expensive than others because they are self-balancing. Most research papers classify SC-MLI by the number of input sources, voltage step-up, and the number of output levels [10,11]. However, voltage fluctuations and the formation of low-frequency harmonics can be affected by both continuous charging and discharging [12]. Overall, a lot of work is being done on 13-level topologies, but since they require multiple input sources and a large component count, the work is somewhat more challenging. Therefore, research initiatives are placing greater emphasis on single-power supply solutions. Similar issues arise in 9-level designs, which have fewer connectors, more auxiliary components, and higher voltage between devices, the same problems come up. This paper proposes a new SC-MLC topology that uses a single power supply consisting of 3 capacitors, 11 switches, and 3 diodes. This allows for the creation of 13 different output voltage levels. By using multiple components at each level, these designs are more efficient than other solutions. The self-balancing feature means that additional balancing circuits are not required, and the single-input structure makes the topology suitable for use in high-voltage networks. The main objective of the research is to develop and experimentally verify a compact and productive SC-MLC architecture that reduces the number of components and complexity of implementation while maintaining the required characteristics. The proposed topology was validated under both low-frequency modulation and PWM operation, and simulation results were in full agreement with experimental findings, clearly demonstrating the advantages of the proposed approach over conventional counterparts.

II. Literature Review or Related Works

Multilevel converters (MLCs) are becoming increasingly valuable as interfaces in renewable energy systems such as photovoltaic (PV) cells and wind turbines. This is because they can generate very good AC waveforms and reduce the load on the electronics caused by high voltages. Early studies focused on standard MLC topologies, including diode-limited configurations, floating capacitors, and cascaded H-bridges, which show that increasing the voltage level results in reduced harmonic distortion and improved sinusoidal output waveform quality. Furthermore, most of these topologies cannot be directly used in low-voltage renewable energy systems. As they require because they require separate DC power supplies or power transformers. Much of the research has focused on improving topologies using switched capacitors (SCs) and switched inductors, i.e., multi-level topologies to boost the DC bus voltage from low-voltage renewable sources. Hu et al. (2021) present a multilevel inverter with switched capacitors, fewer circuit components, and improved voltage scaling capabilities; however, the topology does not achieve a high voltage gain using a single input source. The proposed topology allows for increased output voltage and output levels by using fewer switches, diodes, and capacitors, which means that it can still be used in renewable energy projects. Li (2018) describes a seven-level inverter with only one phase and one DC power supply. The topology employs a set of switched capacitors to triple the input DC voltage. Furthermore, it provides capacitor voltage equalization and prevents overscaling of power switches. Hussan et al. (2023) recently demonstrated a multi-level inverter (TB-SCMLI). However, the topology requires a higher number of power components to achieve similar voltage boosting. It is described as having fewer circuit components and capacitors and self-equalizing the voltage across the switching capacitors, and is designed for renewable energy systems operating at high voltages. These studies indicate that significant improvements can be achieved by significantly reducing the use of DC sources and increasing efficiency. A comparative summary of recent switched-capacitor-based multilevel inverters is presented in Table I I.

III. Methods

The structure of a switched-capacitor multilevel inverter (SC-MLI) is shown in Figure 1. The basic structure consists of a single DC power supply, ten power switches (H_1–H_4, S_1–$S_5, and S_1$), three capacitors ($C_1, C_2, and C_3$), and three separate diodes ($D_1, D_2, and D_3$). This device can produce 13 different output voltage levels with only one DC input. By adding switched capacitors, the system can obtain a threefold the output voltage. The circuit provides energy flow from the DC power supply to both the load and the capacitors through various combinations of switches. The capacitor C_1 is charged directly with the source voltage (VDC), and the capacitors C_2 and C_3 share this voltage equally. The voltages across the capacitors are $VC_1 = VDC, VC_2 = 0.5VDC, and VC_3 = 0.5VDC$. This setup works well for boosting voltage, raising the total output voltage of the main circuit to three times the input source voltage. Here, VDC denotes the input DC source voltage.

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TABLE I
SUMMARY OF RELATED WORKS ON BOOSTING MULTILEVEL INVERTERS

Author(s)	Year	Key Findings	DOI
Hu et al.	2021	Proposed a switched-capacitor-based multilevel inverter with reduced circuit components and voltage boosting capability, suitable for renewable energy applications.	doi:10.1002/2050-7038.12990
Lee	2018	Developed a single-phase, single-source seven-level inverter achieving triple voltage gain with automatic capacitor voltage balancing and low switch voltage stress.	doi:10.1109/ACCESS.2018.2842182
Hussan et al.	2023	Introduced a triple-boost switched-capacitor multilevel inverter (TB-SCMLI) with reduced components and self-voltage-balancing capacitors for sustainable energy systems.	doi:10.1049/pel2.12561

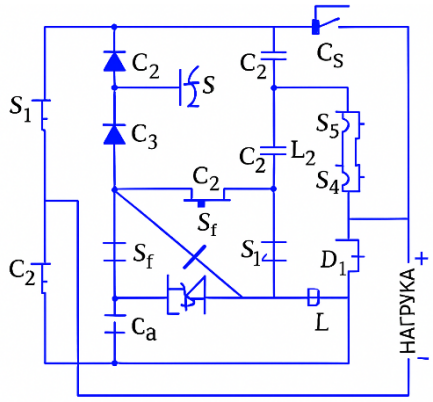

Fig. 1. Multilevel Converter with Triple Voltage Boost

The current flow channels established through the load and capacitors, corresponding to the positive, negative, and zero levels of the output voltage demonstrate the operational principle of the proposed SC-MLI architecture. The red lines representpaths of load current that occur when the capacitors discharge in different switching states. The green lines show the paths of charging current that happen when the capacitors charge. The current path analysis shows that the new SC-MLI topology can provide 13 separate output voltage levels by using only one DC source and adding the voltages of the capacitors in the right order during the right switching sequences. One of the a major challenge capacitor-based multilevel inverters (MLIs) is making sure that the voltage is evenly spread out throughout the capacitors. In many modern topologies, this requires complex control algorithms that keep a watch on capacitor voltages while they are being used. The architecture in this study allows for voltage self-balancing, therefore there is no need for extra balancing circuits or complicated control algorithms. The capacitors in this structure charge and discharge autonomously, which maintains the converter functioning smoothly without any extra systems to balance it out. However, careful selection of capacitance values is required so that the voltage doesn't shift too much. The maximum permissible discharging time (MDT) and the load current during discharging periods are two critical factors that determine the choice of capacitance. If you get the capacitance calculation right, the voltage will be stable no matter what the conditions are.

$$MDT_{C_1} = t_4 - \left(\frac{T}{2} - t_4\right)$$

$$MDT_{C_2} = MDT_{C_3} = t_5 - \left(\frac{T}{2} - t_5\right)$$

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During maximum discharge periods, any variation in the capacitor charge directly affects the amplitude of the output voltage ripple, as expressed in equation (1):

$$\Delta v_{C_i} = \frac{\Delta Q_{C_i}}{C_i} = \frac{1}{C_i} \int_{t_a}^{t_b} i_L \, dt$$

where Δv_{C_i} - is the voltage ripple across capacitor i during the time interval $t_a - t_b$, ΔQ_{C_i} is the amount of charge discharged to the load over this interval, and IL is the load current (which, in this case, coincides with the discharge current). The voltage drop across capacitors during the maximum discharge time (MDT) is calculated as follows [7]:

$$\Delta v_{C1} = \frac{\Delta Q_{C1}}{C_1} = \frac{1}{C_1} \int_{t_4}^{T/2-t_4} i_L \, dt$$

$$\Delta v_{C2} = \frac{\Delta Q_{C2}}{C_2} = \frac{1}{C_2} \int_{t_5}^{T/2-t_5} i_L \, dt$$

$$\Delta v_{C3} = \frac{\Delta Q_{C3}}{C_3} = \frac{1}{C_3} \int_{t_5}^{T/2-t_5} i_L \, dt$$

Since capacitor C_1 discharges within the interval $t_4 - (T/2 - t_4)$, the required capacitance for a given ripple level is determined using equation (2), derived from equations (3) and (4). Similarly, because the maximum discharge duration (MDT) for capacitors C_2 and C_3 is identical, their capacitances are calculated based on the interval $t_5 - (T/2 - t_5)$.

IV. Results and Discussion

MATLAB/Simulink and PLECS were used to create simulation models to test the performance of the proposed SC-MLI topology. To ensure reliability and comparability of results, identical circuit settings were used in both cases. The DC input voltage was set to 60 V, and the capacitance values $C_1 = 2200\,\mu$F, $C_2 = C_3 = 2200\,\mu$F were used for these theoretical calculations. The equivalent series resistance (ESR) of all capacitors was $0.08\,\Omega$. The converter was tested using near-level control (NLC) and sinusoidal pulse width modulation (SPWM) by varying the load, switching frequency, and modulation index (MI). Figure 2(a) shows the simulation results of the NLC model with three different types of loads: purely resistive $(150\,\Omega)$, resistive-inductive $(150\,\Omega + 50\,\text{mH})$, and highly inductive $(150\,\Omega + 200\,\text{mH})$. The output voltage can be varied in 13 different levels, but the current remains constant regardless of the load value. Figure 2(b) shows how the voltage ripple changes when using floating capacitors. The ripple level for each capacitor is always less than 10%. This confirms the correctness of the capacitor selection and the robustness of the proposed architecture.

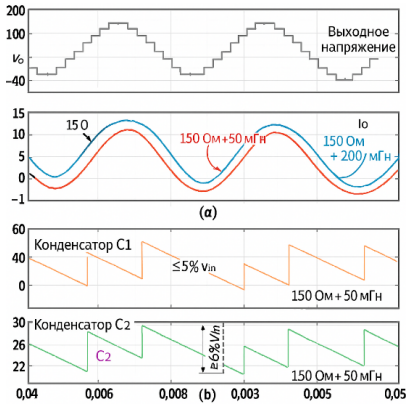

Fig. 2. (a) Output voltage and current for different load conditions; (b) Voltage ripples across capacitors

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The suggested SC-MLI inverter was tested again with a weakly inductive load of $(150\,\Omega + 50\,\text{mH})$, utilizing both SPWM and NLC modulation methods. Harmonic analysis was done to check the quality of the output current. Figure 3(a) shows that the current waveform achieved with SPWM control is close to the ideal sinusoidal reference for the given load conditions. The waveform generated using NLC control also exhibits adequate smoothness. Figure 3(b) shows the harmonic spectra. The total harmonic distortion (THD) of the output current was 1.36 % for SPWM and 2.21 % for NLC. The THD value is a little larger for NLC, but this approach still works because the proposed architecture creates a multilayer output voltage with a high resolution. These results show that the inverter meets the requirements for harmonic distortion without needing high-frequency modulation approaches.

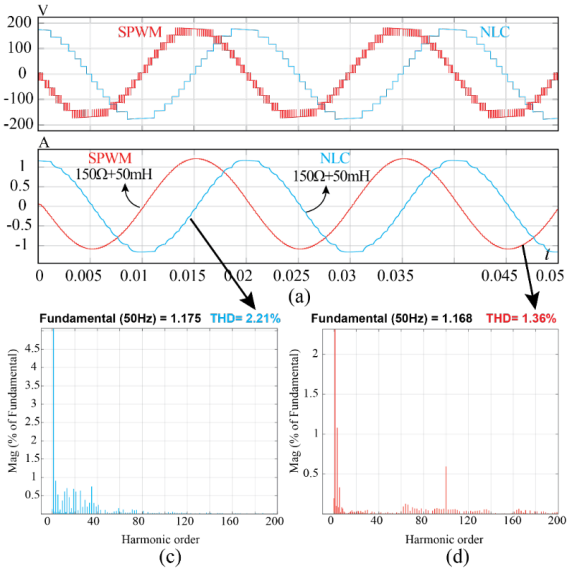

Fig. 3. Performance analysis of the proposed SC-MLI topology under SPWM and NLC control: (a) voltage and current responses; (b) harmonic distortion (THD) evaluation of the output current

Figure 4 illustrates how the proposed 13-level SC-MLI was set up for testing, and Table 4 lists the main sections that were used. A Genesys 2 Kintex-7 FPGA development board sent the power switches their control signals. You could program this board and control the switching accurately. The prototype was tested with both solely resistive and resistive-inductive loads. The inverter's output voltage always had a steady multilayer structure, no matter what the modulation index (MI) or switching frequency was. The results of the simulation and the real-world tests were remarkably similar, which shown that the design was correct and the suggested topology was very reliable.

Using an FPGA, a control platform makes control signals for the Near-Level Control (NLC) method at 50 Hz with a full modulation index. The initial test of the prototype was done with a load of $(150\,\Omega)$. Figure 5(a) illustrates the waveforms for the voltage and current that went with it. Inductors of $50mH$ and $200mH$ were connected in series with the resistive load to see how well the inverter worked with inductive loading. Figures 5(b) and 5(c) exhibit the output characteristics that show how the waveform's quality varies when the load inductance goes up. This demonstrates that the system maintains stable performance even when the load changes.

The influence of modulation index (MI) variation on the inverter's performance is shown in Figure 6. The 13-level SC-MLI was operated sequentially at MI values of 0.3, 0.6, and 1.0, followed by a return to 0.3. The robustness of the control strategy during these changes was demonstrated by the stability and uniformity of the output waveform. Similar to the frequency response analysis, detailed transient interval plots were included to more clearly illustrate the transient behavior.

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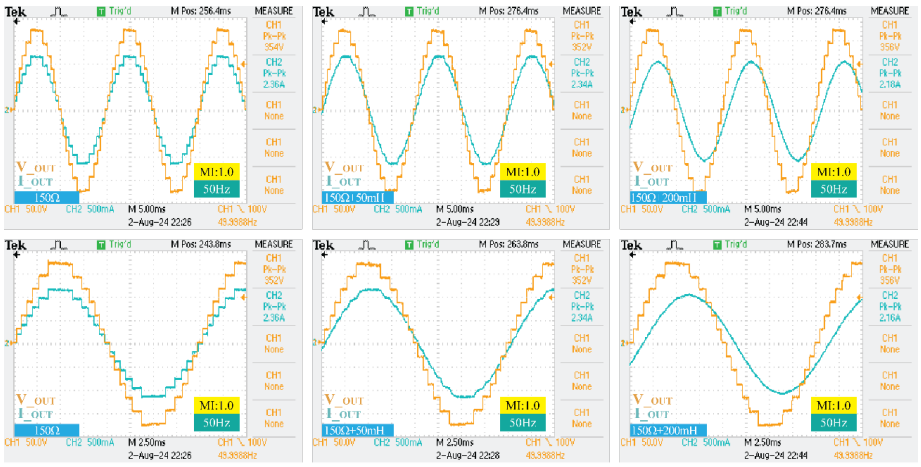

Fig. 4. Experimental evaluation under resistive and resistive–inductive loading: (a) 150 Ω resistive load, (b) (150 Ω + 50 mH) load, (c) (150 Ω + 200 mH) load

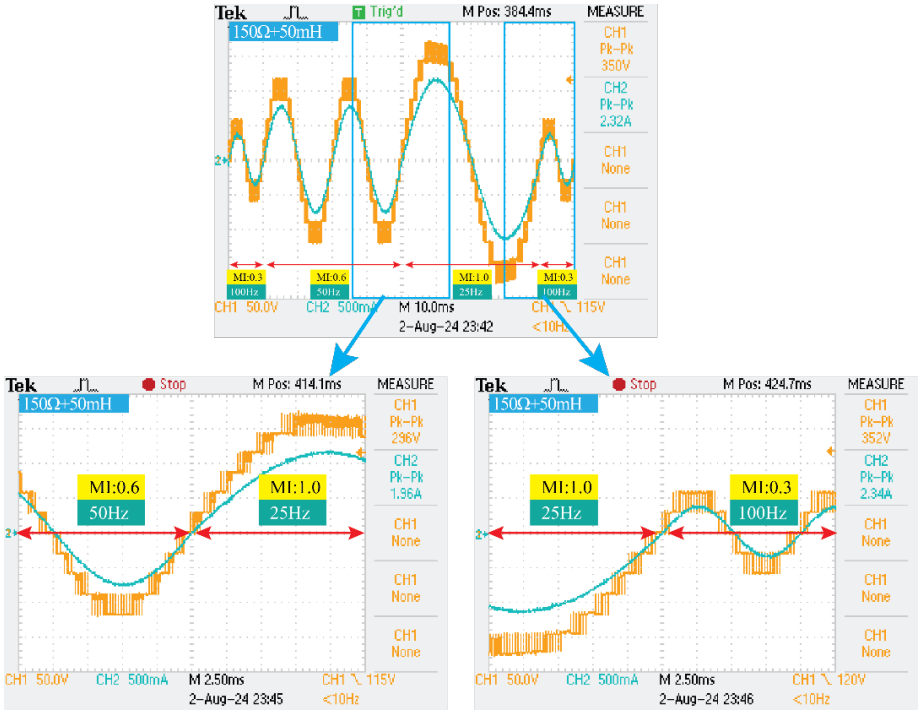

Fig. 5. Output voltage and current response of the proposed 13-level SC-MLI under modulation index and frequency variations

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V. Conclusion and Future Work

In this study, an innovative single-source switched-capacitor multilevel inverter (SC-MLI) architecture is proposed, which can provide 13 discrete voltage levels with a total of three gains. A comparative evaluation is carried out with the state-of-the-art solutions of the last three years, taking into account the main design parameters, including the number of semiconductor switches, the number of coupling capacitors and diodes, the total direct current voltage (TSV), the peak inverse voltage (PIV), and the overall cost efficiency. The results show that the proposed design requires fewer active and passive components compared to common single-source designs, which simplifies implementation, reduces hardware costs, and increases system reliability. Another key advantage is the self-balancing of capacitor voltages, which is achieved without the use of auxiliary sensors or additional control loops. Performance testing was carried out in sinusoidal pulse width modulation (SPWM) and near-level control (NLC) modes. Theoretical analysis, simulation results, and experimental studies consistently confirm the effectiveness of this topology. The results of comprehensive thermal simulations conducted in the PLECS environment showed that the system achieved an efficiency of up to 97.2% in the power range of 100–1000 W. However, during experiments performed in laboratory conditions, it was found that the practical efficiency value was at the level of 95.3%. In addition to meeting the harmonic distortion requirements, the proposed SC-MLI structure provides high energy efficiency despite the small number of elements. This unique combination allows us to consider this topology as a reliable and practical solution for next-generation multi-level inverters.

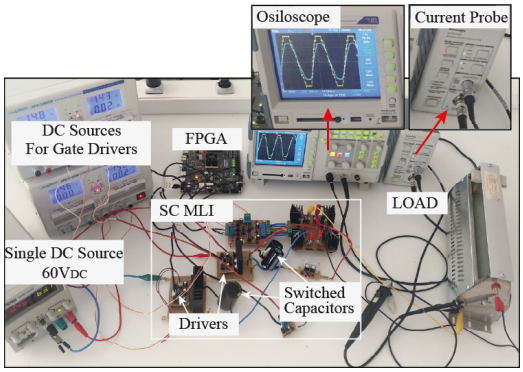

Fig. 6. Laboratory prototype and test bench configuration for the 13-level SC-MLI.

TABLE II
System Parameters and Components

PARAMETERS	
Input Voltage, V_{dc}	60 V
Output Voltage	180 V (peak)
Frequency	50 Hz
Max. Output Power	1000 W
COMPONENTS	
Capacitors	
C1	PG6DI (2200 μF, 600 V, ESR = 80 mΩ)
C2–C3	PG6DI (1200 μF, 600 V, ESR = 80 mΩ)
Power Devices	
IGBT	IGW60N60H3 (V_{CE} = 600 V, I_C = 60 A)
Fast-Recovery Diode	DSEI 60-06 (I_{FAV} = 60 A, V_{RRM} = 600 V, t_{rr} = 35 ns)
Controller	FPGA Development Board (Genesys 2 – Kintex-7)
Output Loads	Resistive (150 Ω), Inductive (50 mH + 200 mH)

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